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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/750,198	12/27/2000	Anil Vasudevan	042390.P9018	7014
7590	04/06/2004			EXAMINER HUYNH, KIM T
R. Alan Burnett BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP 7th Floor 12400 Wilshire Boulevard Los Angeles, CA 90025-1026			ART UNIT 2112	PAPER NUMBER 9
DATE MAILED: 04/06/2004				

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)
	09/750,198	VASUDEVAN, ANIL
	Examiner Kim T. Huynh	Art Unit 2112

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

1) Responsive to communication(s) filed on 08 March 2004.  
 2a) This action is FINAL.                    2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

4) Claim(s) 1-20 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) Claim(s) \_\_\_\_\_ is/are allowed.  
 6) Claim(s) 1-20 is/are rejected.  
 7) Claim(s) \_\_\_\_\_ is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on 27 December 2000 is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
	6) <input type="checkbox"/> Other: _____

## DETAILED ACTION

### ***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Papa et al. (US Patent 6,324,608) in view of Eide et al. (US Patent 6,529,978)

As per claim 1, Papa discloses an apparatus comprising:

- A housing; (fig.1, 101)
- a mainboard (fig.2, 182) including memory (fig.2, 204) and a first processor mounted within the housing; (col.3, lines 61-col.4, line 37)
- a first network interface disposed within the housing and operatively coupled to the first processor, having a first network port (slot) and a first address; (col.4, line 66-col.5, line 10), wherein multiple slots for multiple devices implies different slots per different address)
- at least one expansion slot for receiving a peripheral device; and (col.4, line 66-col.5, line 10)
- a network communications link connecting the first network interface to said at least one expansion slot substantially disposed within the housing; (col.4, line 66-col.5, line 35)

- wherein the first processor is enabled to communicate with a peripheral device adapted to be coupled to one of said at least one expansion slot and having a built-in network interface by transmitting data via the first network interface and the built-in network interface over the network communications link using a network communications on a network transmission protocol. (col.4, line 66-col.6, line 65)

Papa discloses all the limitations as above except using packetized messages based on a network transmission protocol. However, Eide discloses any number of hardware devices coupled to I/O interface 16, an interface to a network 22 to provide communications capability using any number of network protocols (e.g IPX, TCP/IP, SNA, etc.), wherein TCP/IP implies packetized messages. (col.5, lines 10-25)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Eide's teaching into Papa's system so as to have a significant need exists in the art for a manner of changing the bindings between IOA's and IOP's in a hierarchical I/O interface with minimal impact on system availability. (col.2, lines 36-40)

As per claim 2, Papa discloses the apparatus further comprising a second network interface disposed on the mainboard in proximity to one of said at least one expansion slot having a second address and a second network port to enable communication between the first processor and a peripheral device that does not include a built-in network interface when the peripheral device is

mounted in the one of said at least one expansion slots. (col.4, line 66-col.6, line 65)

As per claim 3, Papa discloses wherein the network communications link comprises a network bus embedded in the mainboard. (col.5, lines 21-35), (col.7, lines 7-67)

As per claims 4, 7, Papa discloses wherein the first network interface and the communications link comprise an Ethernet subnet. (col.2, lines 5-24), (col.3, lines 2-10)

As per claim 5, Papa discloses the apparatus further comprising:

- a second processor coupled to the mainboard; and (fig.2, 200s) (col.4, lines 18-37)
- a second network interface operatively coupled to the second processor and the network communications link to enable communication between the second processor and a peripheral device having a built-in network interface when the peripheral device is mounted in one of said at least one expansion slots. (col.4, line 66-col.6, line 65)

As per claim 6, Papa discloses a system comprising a computing machine including:

- A housing; and (fig.1, 101)
- A mainboard to which memory and a first processor are connected, said mainboard providing a first network interface operatively coupled to the

first processor having a first network port and a first address; (col.4, line 66-col.5, line 10)

- A first peripheral disposed within the housing; (col.5, lines 22-col.6, line 65)
- A second network interface operatively coupled to the mainboard, providing a second network port and a second network address, linked in communication with the first peripheral device; and (col.4, line 66-col.6, line 65)
- A communications link between the first and second network interfaces substantially disposed within the housing. (col.4, line 66-col.6, line 65)

Papa discloses all the limitations as above except using packetized messages based on a network transmission protocol. However, Eide discloses any number of hardware devices coupled to I/O interface 16, an interface to a network 22 to provide communications capability using any number of network protocols (e.g IPX, TCP/IP, SNA, etc.), wherein TCP/IP implies packetized messages. (col.5, lines 10-25)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Eide's teaching into Papa's system so as to have a significant need exists in the art for a manner of changing the bindings between IOA's and IOP's in a hierarchical I/O interface with minimal impact on system availability. (col.2, lines 36-40)

As per claim 8, Papa discloses wherein the communication link comprises a network signal bus built into the mainboard. (col.5, lines 22-35)

As per claim 9, Papa discloses wherein the communications link comprises a token ring. (col.2, lines 5-24)

As per claim 10, Papa discloses wherein the second network interface is built into the first peripheral device; (col.3, lines 1-10), wherein interface inherently built-in into peripheral device to provide communication)

As per claim 11, Papa discloses wherein the second network interface is built into the mainboard. (col.3, lines 1-10)

As per claim 12, Papa discloses wherein the peripheral device comprises one of a video subsystem, a memory subsystem, a disk controller and a modem. (col. 4, lines 1-7)

As per claim 13, Papa discloses wherein the mainboard further includes a second processor connected to a third network interface having a third network address and network port connected to the communication link. (col.4, line 66- col.6, line 65)

As per claims 14, 15, 17, Papa discloses a method for enabling communication between a peripheral device disposed within a computing machine having a processor and an application running on the processor, comprising:

- providing a network interface for each of the processor and the peripheral device; (col.4, line 66-col.6, line 65)

- providing a communication link between the network interfaces of the processor and the peripheral device;(col.3, lines 1-10), (col.4, line 66-col.6, line 65)
- creating a network socket for each of the processor and the peripheral device; (col.4, line 66-col.6, line 65)
- stablising a connection between the processor and the peripheral device; and (col.4, line 66-col.6, line 65)
- generating messages with the application; (col.1, line 64-col.23)
- transferring the messages between the processor and peripheral device using a network transmission protocol. (col.1, line 64-col.23)

Papa discloses all the limitations as above except using packetized messages based on a network transmission protocol. However, Eide discloses any number of hardware devices coupled to I/O interface 16, an interface to a network 22 to provide communications capability using any number of network protocols (e.g IPX, TCP/IP, SNA, etc.), wherein TCP/IP inherently implies packetized messages. (col.5, lines 10-25)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Eide's teaching into Papa's system so as to have a significant need exists in the art for a manner of changing the bindings between IOA's and IOP's in a hierarchical I/O interface with minimal impact on system availability. (col.2, lines 36-40)

As per claim 16, Papa discloses the method further comprising applying security measures to determine if an application may connect to a particular peripheral device. (col.1, lines 64-67)

As per claim 18, Papa discloses wherein the communications link and the network interfaces comprise an internal Ethernet network. (col.2, lines 5-24)

As per claim 19, Papa discloses wherein the communications link and the network interfaces comprises an internal token ring network. (col.2, lines 5-24)

As per claim 20, Papa discloses the system further comprising:

A storage device on which software is stored, the software comprising machine instructions that are executable by the first processor that includes a socket application interface (API) that binds the address of the first peripheral device to the second network port and a network interface abstraction layer that provides an abstracted interface that enables an application to communicate with the first peripheral device using a networking protocol. (col.3, lines 1-10), (col.3, line 53-col.4, line55)

***Response to Amendment***

3. Applicant's amendment filed on 3/8/04 have been fully considered but are moot in view of the new ground(s) of rejection.
  - a. In response to applicant's argument that neither Papa and Wadsworth discloses using packetized messages on network protocols. As Eide notes at (col.5, lines 10-25), Eide discloses any number of hardware devices coupled to I/O interface 16, an interface to a network 22 to provide communications capability using any number

of network protocols (e.g IPX, TCP/IP, SNA, etc.), wherein TCP/IP inherently implies packetized messages. Thus, the prior art teaches the invention as claimed and the amended claims do not distinguish over the prior art as applied.

***Conclusion***

4. *Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kim Huynh whose telephone number is (703)305-5384 or via e-mail addressed to [kim.huynh3@uspto.gov]. The examiner can normally be reached on M-F 8:30AM- 6:30PM.*

*If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on (703) 305-4815 or via e-mail addressed to [mark.rinehart@uspto.gov]. The fax phone numbers for the organization where this application or proceeding is assigned are (703)872-9306 for regular communications and After Final communications.*

*Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)306-5631.*

*Kim Huynh*

Kim Huynh  
April 1, 2004

*Khanh Dang*  
Primary Examiner